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DICKE, BILLIG & CZAJA, P.L.L.C.
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,172	BHARDWAJ, SANJAY	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29 and 46* is/are allowed.

6)☒ Claim(s) *23-28,30-45,47-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. An objection to the title of the invention is withdrawn since it is being amended accordingly.

2. Claim objections, on claims 25,26,35 and 42 are withdrawn since they are being amended accordingly.

3. Claims 23-28,30-45 and 47-49 are rejected by the same ground of rejections.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 23-25, 30-32, 34-36, 39-41, 43,47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan (U.S. 5,638,3697) in view of Bayliss (U.S. 4,407,016).

Regarding claim 40, Gaytan'367 discloses an apparatus (see FIG. 6) for interfacing a digital data processor (see FIG. 3, Host System 390 process the data; see col. 3, lines 39-41) to a digital communication network (see FIG. 3, ATM Network Media 400; see col. 3, lines 43-44), comprising:

a first data port (see FIG. 3, the combined system of system I/O bus 380 and System Bus Interface 200) that permits exchange of digital data with the data processor (see col. 3,

lines 38-50; note that the combined system permits/allows data exchange/transmission with the host system 390);

a second data port (see FIG. 3, media interface 320) that permits exchange of digital data with the communication network (see col. 3, lines 62-67; note that the interface permits/allows data exchange/transmission with the external ATM network 400); and

a data alignment apparatus (see FIG. 6b, Byte Packing Circuit 650) coupled between said first and second data ports (see FIG. 3, note that byte packing circuit is between the combined system of system I/O bus 380 and System Bus Interface 200, and Media interface 320),

including an input (see FIG. 6b, Input Storage Element 660) for receiving an input temporal series of parallel-formatted input groups of digital data units (see col. 7, lines 20-27; note that input element 660 receives the input series/serial of parallel-formatted (i.e. word packing/formatted) groups/segments/pre-defined-portion of data from the word packing circuit),

a data aligner (see FIG. 6b, a combined system of Save Storage Element 665, Selector/combiner 675 and Byte Rotate Circuit 655) coupled to said input and responsive to said input series for producing an output temporal series of parallel-formatted output groups of said digital data units (see FIG. 6b, PDATA towards TX buffer memory; see col. 7, lines 20-31; note that in response to receiving input data, the combined system of save Storage Element 665 and Selector 675 transmits the output series/serial of parallel-formatted (i.e. word/byte packing/formatted) groups/segments/pre-defined-portion of data towards the TX buffer), and

an output (see FIG. 6b, Output Storage Element 670) coupled to said data aligner for outputting said output series (see FIG. 6b, note that Output element 670 couples to the combined system of Save Storage Element 665 and Selector 675 and outputs the data towards TX buffer memory);

said data aligner including a buffer (see FIG. 6b, Save Storage Element 665) coupled to said input (see FIG. 6b, Input Element 660) for storing data units of a first said input group (see FIG. 7c; Save/Store/Buffer Element 665 stores/saves data (i.e. data 1 and 2) of 1st input cycle of bytes/group) while a second said input group is received at said input (see FIG. 7c; note that data 1-2 stores in the Save element 665 while 2nd /next input cycle of bytes/group (i.e. data 3-6) is received at Input Element 660); see col. 9, , lines 40-48; and

a combiner (see FIG. 6b, a Selector 657 combines/multiplexes the output data from both Input Element 660 and Save element 665) coupled to said buffer (see FIG. 6b, Save Storage Element 665) and said input (see FIG. 6b, Input element 660) for producing one of said output groups (see FIG. 7d, one of the output bytes/group (i.e. data 1-4)) by combining in parallel format (see FIG. 7d, note that output element 670 combines/multiplexes in parallel format (i.e. four parallel inputs to one serial output)) all of said data units stored in said buffer (see FIG. 7c, all data unit previously stored in Save/buffer element 665 (i.e. data 1-2)) and selected data units of said second input group (see FIG. 7c, note that data 3-4 from 2nd/next cycle of bytes/group is selected in order to combine/multiplex); see col. 9, lines 40-52; see FIG. 8, steps 115-130; and

said data alignment apparatus including a data path coupled to said combiner and said output (see FIG. 6b, a path that couples to Input element 660, Selector 675 and Output

element 670) for permitting said one output group to be transferred to said output (see FIG. 7c-d; note that data 3-4 byte/group is directly transferred from input element to output element via the a direct path.)

Gaytan'367 does not explicitly disclose transferring to said output without being stored in said buffer.

However, the above-mentioned claimed limitations are taught by Bayliss'016. In particular, Bayliss'016 teaches transferring to said output without being stored in said buffer (see col. 2, lines 25-31; note that the data is transferred/outputted to a single address by bypassing the buffer).

In view of this, having the system of Gaytan'367 and then given the teaching of Bayliss'016, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Gaytan'367, for the purpose of bypassing the buffer during data transfers, as taught by Bayliss'016, since Bayliss'016 states the advantages/benefits at col. 2, lines 15-20, 26-30, that it would improve the data transfer process by allowing the data to bypass. The motivation being that by bypassing the buffer, it can reduce the delay and improve the data transfer process.

Regarding claim 41, Gaytan'367 discloses wherein said combiner is for parallel concatenating (see FIG. 7d, output element 670 combines/multiplexes/concatenates in parallel format (i.e. four parallel inputs to one serial output)) said selected data units of said second input group (see FIG. 7c, note data 3-4 from 2nd/next cycle of bytes/group is selected in order to combine/multiplex) with all of said data units stored in said buffer (see FIG. 7c, all data unit previously stored in Save/buffer element 665 (i.e. data 1-2)) to produce said one

output group (see FIG. 7d, one of the output bytes/group (i.e. data 1-4); see col. 9, lines 40-52; see FIG. 8, steps 115-130.

Regarding claim 43, Gaytan'367 discloses wherein said combiner includes a selector (see FIG. 6b, a Selector 657) having inputs respectively coupled to said first-mentioned input (see FIG. 7d, note that Selector 670 have two data inputs lines couple in parallel format to each data input line of input element 660) and said buffer (see FIG. 7d, note that Selector 670 have two data inputs lines couple in parallel format to each data line of save/buffer element 665), and having an output coupled to said data path (see FIG. 7d, an output bytes/group (i.e. data 1-4) is coupled to a path); see col. 9, lines 40-52; FIG. 8, steps 115-130.

Regarding claim 47, Gaytan'367 discloses provided as one of a SONET card, an Ethernet card and a token ring card (see col. 3, lines 30-45; note that NIC card can be Ethernet or Token Ring card utilized in Ethernet or Token Ring network 160).

Regarding claim 48, the combined system of Gaytan'367 and Bayliss'016 discloses all aspects of the claimed invention set forth in the rejection of Claim 40 as described above. Bayliss'016 discloses said data path bypasses said buffer (see col. 2, lines 25-31; note that the data is transferred/outputted to a single address by bypassing the buffer). In view of this, having the system of Gaytan'367 and then given the teaching of Bayliss'016, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Bayliss'016, by bypassing the buffer, as taught by Bayliss'016, for the same motivation as stated above in Claim 40 above.

Regarding claim 23, the apparatus claim, which has substantially disclose all the limitations of the respective apparatus claim 40. Therefore, it is subjected to the same rejection.

Regarding claim 24, the apparatus claim, which has substantially disclose all the limitations of the respective apparatus claim 41. Therefore, it is subjected to the same rejection.

Regarding claim 25, the apparatus claim, which has substantially disclose all the limitations of the respective apparatus claim 43. Therefore, it is subjected to the same rejection.

Regarding claim 30, Gaytan'367 discloses wherein each said input group is one of a head element, a body element and a tail element of a data packet (see col. 4, lines 6-10, 29-39,40-61; note that each input/output group/byte is one of header/tailor and data/payload of the data packet. Also, it is well known in the art that the packet must have a header/tailor and data/payload in order to transmit/receive over the data/packet communication network).

Regarding claim 31, Gaytan'367 discloses wherein each of said data units is a byte (see FIG. 3, Byte packing circuit; thus, it is clear that each of data units is a byte).

Regarding claim 32, Gaytan'367 discloses wherein said buffer has a maximum data unit storage capacity (see FIG. 7a, Storage/Buffer Element 665 has maximum of four storage capacity) that is equal to a maximum data unit capacity of the input groups in said input series (see FIG. 7a, Input Element 660 has four maximum data capacity of the input groups/bytes in series of input); see col. 9, lines 10-45.

Regarding claim 34, the claim, which has substantially disclose all the limitations of the respective apparatus claim 48. Therefore, it is subjected to the same rejection.

Regarding Claim 35, the method claim (see FIG. 8, an operational steps/method of data packing circuits in FIG. 6), which has substantially disclose all the limitations of the respective apparatus claim 40. Therefore, it is subjected to the same rejection.

Regarding claim 36, the method claim, which has substantially disclose all the limitations of the respective apparatus claim 41. Therefore, it is subjected to the same rejection.

Regarding claim 39, the claim, which has substantially disclose all the limitations of the respective apparatus claim 48. Therefore, it is subjected to the same rejection.

6. Claim 26, 27, 37,42,44 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan'367 and Bayliss'016, as applied to claim 23, 35 and 40 above, and further in view of Roskowski (U.S. 5,410,677).

Regarding claim 26, Gaytan'367 discloses wherein said combiner comprises a rotator (see FIG. 6b, a rotating function within the Selector 657) for rotating the data units of said second input group (see col. 8, lines 1-20; note that the selector performs the rotating the data of input group/byte based upon the instruction 656 form the rotator 655, thus, it is a rotator) to position said selected data units of said second input group for said combiner (FIG. 7c, note data 3-4 from 2nd/next cycle of bytes/group is positioned and selected by the selector/combiner) to parallel concatenate said selected data units (see FIG. 7d, note that Selector 670 have two data inputs lines (i.e. data lines 3 and 4) from data input line of input

element 660, which can be combined/concatenated in parallel format) with all of said data units stored in said buffer (see FIG. 7c, all data unit previously stored in Save/buffer element 665 (i.e. data 1-2)) to produce said one output group (see FIG. 7d, one of the output bytes/group (i.e. data 1-4)); see col. 9, lines 40-52; see FIG. 8, steps 115-130.

Neither Gaytan'367 nor Bayliss'016 explicitly discloses a rotator coupled to said input.

However, the above-mentioned claimed limitations are taught by Roskowski'677. In particular, Roskowski'677 teaches a rotator (see FIG. 3, Rotator 18 and/or see FIG. 5, Rotator 35) coupled to said input (see FIG. 3, Input/Buffer/Register 17) for rotating the data units (see FIG. 5, Address/Data Input data 64) of said second input group (see FIG. 5, Address/Data Input 33) to position said selected data units of said second input group (see col. 6, lines 19-30, 51-56; col. 8, lines 23-40, see col. 9, lines 60-67; note that the rotator couples to the input and the combiner/multiplexer and rotates the data of input group/byte).

In view of this, having the combined system of Gaytan'367 and Bayliss'016, then given the teaching of Roskowski'677, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Gaytan'367 and Bayliss'016, for the purpose of providing a rotator that coupled to input, as taught by Roskowski'677, since Roskowski'677 states the advantages/benefits at col. 2, lines 1-20 that it would reduce the overall cost of the computer system by translating/rotating data from one format to the other. The motivation being that by rotating/translating data from one format to other, it can reduce the cost and increase the efficiency since both format are now interoperate-able via one system.

Regarding claim 27, Gaytan'367 discloses wherein said data aligner includes a controller (see FIG. 6b, Byte Rotate Circuit 655 which has controlling/processing functionality means to instruct/process Selector 675) for determining a rotation amount by which said rotator is to rotate the data units of said second input group (see FIG. 6b, Byte Rotate Circuit determines/computes the rotation amount/value, by utilizing pipe count and buffer addr, to rotate the data of 2nd input cycle bytes/group; see col. 8, lines 4-20),

said controller having an output (see FIG. 6b, Rotational Select Line 656) coupled to said rotator for providing to said rotator information indicative of said rotation amount (see FIG. 6b, Byte Rotate Circuit 655, which couples to Selector 675 with the rotating functionality means, instructs the rotating functionality means with the rotation amount/value to rotate the data; see col. 8, lines 4-20).

Regarding Claim 37, the claim, which has substantially disclose all the limitations of the respective claim 26. Therefore, it is subjected to the same rejection.

Regarding Claim 42, the claim, which has substantially disclose all the limitations of the respective claim 26. Therefore, it is subjected to the same rejection.

Regarding Claim 44, the claim, which has substantially disclose all the limitations of the respective claim 27. Therefore, it is subjected to the same rejection.

Regarding new Claim 49, Gayton discloses a data alignment apparatus (see FIG. 6), comprising:

an input (see FIG. 6b, Input Storage Element 660) for receiving an input temporal series of parallel-formatted input groups of digital data units (see col. 7, lines 20-27; note that input element 660 receives the input series/serial of parallel-formatted (i.e. word

packing/formatted) groups/segments/pre-defined-portion of data from the word packing circuit),

a data aligner (see FIG. 6b, a combined system of Save Storage Element 665, Selector/combiner 675 and Byte Rotate Circuit 655) coupled to said input and responsive to said input series for producing an output temporal series of parallel-formatted output groups of said digital data units (see FIG. 6b, PDATA towards TX buffer memory; see col. 7, lines 20-31; note that in response to receiving input data, the combined system of save Storage Element 665 and Selector 675 transmits the output series/serial of parallel-formatted (i.e. word/byte packing/formatted) groups/segments/pre-defined-portion of data towards the TX buffer), and

an output (see FIG. 6b, Output Storage Element 670) coupled to said data aligner for outputting said output series (see FIG. 6b, note that Output element 670 couples to the combined system of Save Storage Element 665 and Selector 675 and outputs the data towards TX buffer memory);

said data aligner comprsing:

a buffer (see FIG. 6b, Save Storage Element 665) coupled to said input (see FIG. 6b, Input Element 660) for storing data units of a first said input group (see FIG. 7c; Save/Store/Buffer Element 665 stores/saves data (i.e. data 1 and 2) of 1st input cycle of bytes/group) while a second said input group is received at said input (see FIG. 7c; note that data 1-2 stores in the Save element 665 while 2nd /next input cycle of bytes/group (i.e. data 3-6) is received at Input Element 660); see col. 9, , lines 40-48; and

a selector (see FIG. 6b, a Selector 657 combines/multiplexes the output data from both Input Element 660 and Save element 665) coupled to said buffer (see FIG. 6b, Save Storage Element 665) and said input (see FIG. 6b, Input element 660), and having an output coupled to a data path (see FIG. 6b, a path that couples to Input element 660, Selector 675 and Output element 670), said data path coupled to said output for permitting said one output group to be transferred to said output (see FIG. 7c-d; note that data 3-4 byte/group is directly transferred from input element to output element via the a direct path; see col. 9, lines 40-52).

a rotator (see FIG. 6b, a rotating function within the Selector 657) for rotating the data units of said second input group (see col. 8, lines 1-20; note that the selector performs the rotating the data of input group/byte based upon the instruction 656 form the rotator 655, thus, it is a rotator) to position said selected data units of said second input group (FIG. 7c, note data 3-4 from 2nd/next cycle of bytes/group is positioned and selected by the selector/combiner) to parallel concatenate said selected data units (see FIG. 7d, note that Selector 670 have two data inputs lines (i.e. data lines 3 and 4) with all of said data units stored in said buffer (see FIG. 7c, all data unit previously stored in Save/buffer element 665 (i.e. data 1-2)) to produce said one output group (see FIG. 7d, one of the output bytes/group (i.e. data 1-4)); see col. 9, lines 40-52; see FIG. 8, steps 115-130;

a controller (see FIG. 6b, Byte Rotate Circuit 655 which has controlling/processing functionality means to instruct/process Selector 675) for determining a rotation amount by which said rotator is to rotate the data units of said second input group (see FIG. 6b, Byte Rotate Circuit determines/computes the rotation amount/value, by utilizing pipe count and buffer addr, to rotate the data of 2nd input cycle bytes/group; see col. 8, lines 4-20), said

controller having an output (see FIG. 6b, Rotational Select Line 656) coupled to said rotator for providing to said rotator information indicative of said rotation amount (see FIG. 6b, Byte Rotate Circuit 655, which couples to Selector 675 with the rotating functionality means, instructs the rotating functionality.

Gaytan'367 does not explicitly disclose transferring to said output without being stored in said buffer.

However, the above-mentioned claimed limitations are taught by Bayliss'016. In particular, Bayliss'016 teaches transferring to said output without being stored in said buffer (see col. 2, lines 25-31; note that the data is transferred/outputted to a single address by bypassing the buffer).

In view of this, having the system of Gaytan'367 and then given the teaching of Bayliss'016, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Gaytan'367, for the purpose of bypassing the buffer during data transfers, as taught by Bayliss'016, since Bayliss'016 states the advantages/benefits at col. 2, lines 15-20, 26-30, that it would improve the data transfer process by allowing the data to bypass. The motivation being that by bypassing the buffer, it can reduce the delay and improve the data transfer process.

Neither Gaytan'367 nor Bayliss'016 explicitly discloses a rotator coupled to said input.

However, the above-mentioned claimed limitations are taught by Roskowski'677. In particular, Roskowski'677 teaches a rotator (see FIG. 3, Rotator 18 and/or see FIG. 5, Rotator 35) coupled to said input (see FIG. 3, Input/Buffer/Register 17) for rotating the data units

(see FIG. 5, Address/Data Input data 64) of said second input group (see FIG. 5, Address/Data Input 33) to position said selected data units of said second input group (see col. 6, lines 19-30, 51-56; col. 8, lines 23-40, see col. 9, lines 60-67; note that the rotator couples to the input and the combiner/multiplexer and rotates the data of input group/byte).

In view of this, having the combined system of Gaytan'367 and Bayliss'016, then given the teaching of Roskowski'677, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Gaytan'367 and Bayliss'016, for the purpose of providing a rotator that coupled to input, as taught by Roskowski'677, since Roskowski'677 states the advantages/benefits at col. 2, lines 1-20 that it would reduce the overall cost of the computer system by translating/rotating data from one format to the other. The motivation being that by rotating/translating data from one format to other, it can reduce the cost and increase the efficiency since both format are now interoperate-able via one system.

7. Claim 28,33,38 and 45 rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan'367 and Bayliss'016, as applied to claim 23 and 32 above, and further in view of well established teaching in art.

Regarding claim 28, the combined system of Gaytan'367 and Bayliss'016 discloses wherein said controller determines said rotation amount as described above in claims 27,37, and 44. Gaytan'367 teaches wherein said buffer has a maximum data unit storage capacity (see FIG. 7a, Storage/Buffer Element 665 has maximum of four storage capacity).

Neither Gaytan'367 nor Bayliss'016 explicitly disclose rotating based on a data unit storage capacity of said buffer (per well established teaching in art, it is well known in the art that the buffer/memory/storage capacity must be defined, and the rotation must be performed according to size/capacity of the buffer/memory/storage).

However, the above-mentioned claimed limitations are taught by well-established teaching in art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Gaytan'367 and Bayliss'016, as taught by well established teaching in art for the purpose of rotating according to the size/capacity of the buffer/memory. The motivation being that by rotating according to the size/capacity of the buffer/memory, it can reduce the disadvantage of over-rotation (i.e. over writing the valid data), under-rotation (i.e. leaving invalid/null/empty data), or data being out-of-sequence.

Regarding claim 33, the combined system of Gaytan'367 and Bayliss'016 discloses wherein said maximum data unit storage capacity of said buffer as described above in claims 23 and 32.

Neither Gaytan'367 nor Bayliss'016 explicitly disclose the capacity of said buffer is 16 data units (per well established teaching in art, it is well known in the art that the buffer/memory/storage can be designed with the capacity of 16 data units).

However, the above-mentioned claimed limitations are taught by well-established teaching in art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Gaytan'367 and Bayliss'016, as taught by well established teaching in art for the purpose of designing a buffer with a

capacity of 16 data unit. The motivation being that by setting/designing a specific buffer capacity/size, it can reduce the buffer over-flow or over-allocation.

Regarding Claim 38, the claim, which has substantially disclose all the limitations of the respective claim 28. Therefore, it is subjected to the same rejection.

Regarding Claim 45, the claim, which has substantially disclose all the limitations of the respective claim 28. Therefore, it is subjected to the same rejection.

Allowable Subject Matter

8. Claims 29 and 46 are allowed.

Response to Arguments

9. Applicant's arguments filed 8-30-2004 have been fully considered but they are not persuasive.

Regarding claims 23,35, and 40, the applicant argued that, "...the examiner conceded that Gaytan does not disclose a data path coupled to said combiner and said output for permitting said one output group...(see Office Action page 5)..." in page 13, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees that the examiner conceded that Gaytan does not disclose a data path coupled to said combiner and said output for permitting said one output group. The first office action page 5 (as indicated by the applicant) does not state or suggest that examiner is conceding regarding above argued limitation. What the examiner concedes, as clearly stated in page 5, paragraph 4 of the first office, is "Gayton'367 does not explicitly disclose transferring to said output without being

stored in said buffer". Thus, it is clear that examiner conceding does not include the applicant argued limitations.

Regarding claims 23-28, 30-45,47-49, the applicant argued that, "...Bayliss does not discloses a data path coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer..." in page 13, paragraph 3; page 14, paragraph 4.

In response to applicant's argument, the examiner respectfully disagrees that Bayliss does not discloses a data path coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As recited in the first office action, Gayton discloses a data path coupled to said combiner (see FIG. 6b, a Selector 657 combines/multiplexes the output data from both Input Element 660 and Save element 665) and said output (see FIG. 6b, Input element 660) for permitting said one output group to be transferred to said output (see FIG. 7c-d; note that data 3-4 byte/group is directly transferred from input element to output element via the a direct path; see col. 9, lines 40-52.) Bayliss discloses transferring to said output without being stored in said buffer (see col. 2, lines 25-31; note that the data is transferred/outputted

to a single address by bypassing the buffer). Thus, it clear that the combined system of Gayton and Bayliss clearly discloses the argued limitations.

Regarding claims 23-28, 30-45,47-49, the applicant argued that, "...the buffer in Bayliss is not coupled to a combiner and an output for permitting an output group to be transferred to the output without being stored in the buffer...the buffer in Bayliss serves a different purpose and performances a different function than the buffer in the present invention..." in page 13, paragraph 3.

In response to applicant's argument as described above, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Examiner is <u>not</u> bodily incorporating or replacing any of the structure (i.e. buffer or any other) of the Gayton with Bayliss. Examiner is reciting the "teaching" of Bayliss.

Moreover, the examiner is reciting the teaching of Bayliss for applicant's <u>negative</u> claimed limitation, "**transferring to said output without being stored in said buffer**". What applicant claim is the transferring data to the output without being stored in the buffer. Thus, Bayliss clearly teaches the claimed limitation of transferring data to the output without being stored in the buffer, that is, by bypassing or not using the buffer when transmitting/transferring data to output (see above response).

Regarding the argument Bayliss's buffer serving a different purpose and performs since a different function than the invention, the examiner is not replacing or bodily incorporating Gayton's buffer with Bayliss' buffer for combination. Thus having Bayliss's buffer having "a different purposes and function" than the invention, is irrelevant.

Regarding claims 23-28, 30-45,47-49, the applicant argued that, "...one skilled in the art could not combine the teaching of Gayton and Bayliss ..." in page 13, paragraph 3, Gayton and Bayliss fails to teach or suggest such combination..." in page 13, paragraph 4 and page 13, paragraph 4.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation is clearly disclosed in Bayliss at col. 2, line 15-20,26-30, that such modification would improve the data transfer process by allowing the data to bypass, and by bypassing the buffer, it can reduce the delay and improve the data transfer process.

Regarding claims 23-28, 30-45,47-49, the applicant argued that, "...Bayliss does not relate to a data alignment apparatus..." in page 14, paragraph 1.

In response to applicant's argument that Bayliss's does not relate to a data alignment apparatus, the examiner is not replacing or bodily incorporating Gayton's data

alignment with Bayliss' data alignment for combination. Thus, Bayliss's having or not having "a data alignment apparatus" is irrelevant. Moreover, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the combination of references as set forth in the 103 rejections is proper, thus, Claims 23-28, 30-45,47-49 are obvious over Gayton in view of BBayliss for at least the reasons discussed above.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
2/28/05

BOB PHUNKULH
PRIMARY EXAMINER